

**MYERS BIGEL SIBLEY & SAJOVEC**

**Patent Attorneys**

**4140 Parklake Avenue, Suite 600  
Raleigh, North Carolina 27612 USA**

**or**

**P.O. Box 37428  
Raleigh, North Carolina 27627 USA**

**Tel: (919) 854-1400**

**Fax: (919) 854-1401**

**RECEIVED  
CENTRAL FAX CENTER**

**MAR 30 2005**

**TELECOPIER TRANSMISSION  
COVER SHEET**

**Date: March 30, 2005**

**File Number: 5649-927DV**

**Telecopier No.: 703-872-9306**

**To: Commissioner for Patents  
Examiner: Toniae M. Thomas  
Group Art Unit: 2822**

**Company: United States Patent and Trademark Office**

**From: Elizabeth A. Stanek**

**Number of Pages: 4  
(including cover)**

**Return fax to: Erin Campion**

If there is a problem with this transmission, please call (919) 854-1400.  
Our fax number is (919) 854-1401.

**Confidentiality Note**

The information contained in this facsimile message is legally privileged and confidential information intended only for the use of the individual or entity named above. If the reader of this message is not the intended recipient, you are hereby prohibited. If you have received this telecopy in error, please immediately notify us by telephone and return the original message to us at the address above via the United States Postal Service. THANK YOU.

MAR 30 2005

Attorney Docket No. 5649-927DV

PATENT

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Hyoung-Joon Kim et al.

Confirmation No.: 7889

Serial No.: 10/706,647

Group Art No.: 2822

Filed: November 12, 2003

Examiner: Toniae M. Thomas

For: METHODS OF FABRICATING INTEGRATED CIRCUIT DEVICES PROVIDING  
IMPROVED SHORT PREVENTION

March 30, 2005

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

## INTERVIEW SUMMARY

Applicants concur with the Interview Summary provided by the Examiner. In particular, on February 2, 2005, Applicants' representative, Elizabeth A. Stanek, was contacted by Examiner Thomas regarding a proposed Examiner's Amendment to place the claims in the present application in condition for allowance. During the interview, Applicants' representative and the Examiner discussed Independent Claims 1, 5 and 9 and reached agreement that the claims should be amended as follows:

1. A method of fabricating an integrated circuit device comprising:  
forming a conductive layer on a microelectronic substrate;  
forming a first insulating layer on the conductive layer, the first insulating layer including an overhanging portion that extends beyond the conductive layer;  
forming a second insulating layer on the microelectronic substrate to cover the first insulating layer; and  
etching the second insulating layer to form a sidewall insulating region disposed laterally adjacent a sidewall of the conductive layer and extending between the overhanging portion of the first insulating layer and the microelectronic substrate, such that a portion of the second insulating layer remains on an upper surface of the first insulating layer.

5. A method of fabricating a self-aligned contact structure for a microelectronic device, the method comprising:  
forming a conductive layer on a microelectronic substrate;  
forming a first insulating layer on the conductive layer, the first insulating layer including an overhanging portion that extends beyond the conductive layer;  
forming a second insulating layer on the microelectronic substrate to cover the first insulating layer;  
etching the second insulating layer to form a sidewall insulating region disposed laterally adjacent a sidewall of the conductive layer and extending between the overhanging portion of the first insulating layer and the microelectronic substrate, such that a portion of the second insulating layer remains on an upper surface of the first insulating layer; and

In re: Kim et al.  
Serial No.: 10/706,647  
Filed: November 12, 2003  
Page 2

forming a conductive region disposed laterally adjacent to the sidewall insulating region such that the sidewall insulating region separates the sidewall of the conductive layer and the conductive region.

9. A method of fabricating an integrated circuit memory device, comprising:  
forming a first bit line comprising:  
forming a first conductive layer on a microelectronic substrate; and  
forming a first insulating layer on the first conductive layer, the first insulating layer including a first overhanging portion that extends beyond the first conductive layer; and  
forming a second bit line comprising:  
forming a second conductive layer on the microelectronic substrate;  
and  
forming a second insulating layer on the second conductive layer, the second insulating layer including a second overhanging portion that extends beyond the second conductive layer;  
forming a third insulating layer on the microelectronic substrate to cover the first and second bit lines; and  
etching the third insulating layer to simultaneously form a first sidewall insulating layer region disposed laterally adjacent to a first sidewall of the first conductive layer, and a second sidewall insulating region disposed laterally adjacent to a second sidewall of the second conductive layer, wherein the first sidewall insulating region extends between the first overhanging portion of the first insulating layer and the microelectronic substrate, and the second sidewall insulating region extends between the second overhanging portion of the second insulating layer and the microelectronic substrate, such that a portion of the third insulating layer remains on an upper surface of the first insulating layer and an upper surface of the second insulating layer.

Applicants' representative and the Examiner reached agreement that the above claims recite patentable subject matter and would place the case in condition for allowance. Accordingly, Applicants' representative authorized the Examiner to enter an Examiner's Amendment amending the claims, as shown above, thereby placing the case in condition for allowance.

Respectfully submitted,



Elizabeth A. Stanek  
Registration No. 48,568  
Attorney for Applicants

MAR. 30. 2005 5:00PM

MBS&S 919 854-1401

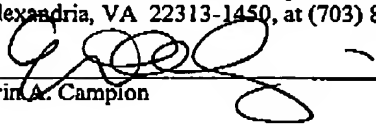
NO. 3555 P. 4

In re: Kim et al.  
Serial No.: 10/706,647  
Filed: November 12, 2003  
Page 3

**USPTO Customer No. 20792**  
Myers Bigel Sibley & Sajovec, P.A.  
P. O. Box 37428  
Raleigh, North Carolina 27627  
Telephone: (919) 854-1400  
Facsimile: (919) 854-1401

**CERTIFICATE OF FACSIMILE TRANSMISSION**

I hereby certify that this correspondence is being sent by facsimile transmission to Commissioner for Patents, Alexandria, VA 22313-1450, at (703) 872-9306 on March 30, 2005.

  
\_\_\_\_\_  
Erin A. Campion